I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as First Class Mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Dated: _____ Signature: _____
(Maureen Divito)

Docket No.: 1801270.00126US1
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Jason Souloglou et al.   Confirmation No.: 5766

Application No.: 09/828,049   Art Unit: 2192

Filed: April 6, 2001   Examiner: C. C. Chow

Title: PROGRAM CODE CONVERSION

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PROPOSED AMENDMENT IN RESPONSE TO EXAMINER'S REQUEST

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Examiner's request, please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

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Application No. 09/828,049   Docket No.: 1801270.00126US1
Amendment dated March 13, 2007
Amendment in Response to Examiner's Request

AMENDMENTS TO THE CLAIMS

This listing of the claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method of generating an intermediate representation of a register-based program code written for running on a programmable machine having a set of registers, wherein the set of registers include at least one variable size register which is addressable by the program code in a plurality of different widths, the method comprising the computer-implemented steps of:

generating a plurality of register objects each representing a respective one of the registers as referenced by the program code, wherein the at least one variable size register is represented by an associated set of the register objects having one of the register objects for each different width of the variable size register;

generating a plurality of expression objects each representing a respective operator or operand in the program code relating to the registers; and

forming a network of the register objects and the expression objects, wherein each of the expression objects is referenced by one or more of the register objects to which it relates.

2. (Previously presented) The method according to claim 1, wherein a write operating in the program code to the variable size register at a particular width is represented in the intermediate representation by writing to the register object corresponding to the appropriate width and maintaining a record of which of the register objects contain valid data.

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3. (Previously presented) The method according to claim 2, wherein a read operation from a variable sized register is represented in the intermediate representation by determining from the record if there is valid data in more than one corresponding register object which must be combined to give the same effect as reading from the variable size register, and

(i)   if it is determined that no such combination is required, reading from the appropriate register object; and

(ii)   if it is determined that such combination is required, combining the contents of appropriate register objects to provide a real value.

4. (Previously presented) The method of claim 1, further comprising translating the program code written for execution by a processor of a first type so that the program code may be executed by a processor of a second type, using the generated intermediate representation.

5. (Previously presented) The method of claim 4, wherein the translating step is performed dynamically as the program code is run.

6. (Previously presented) The method of claim 1, further comprising optimizing the program code by optimizing the generated intermediate representation.

7. (Previously presented) The method of claim 6, wherein the optimizing step is used to optimize the program code written for execution by a processor of a first type so that the program code may be executed more efficiently by that processor.

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8. (Previously presented) A method of generating an intermediate representation of program code expressed in terms of an instruction set of a subject processor comprising at least one variable size register which is accessible by the program code in a plurality of different field widths, the method comprising the computer implemented steps of:

generating a set of associated register objects each representing a different field width of the variable size register;

for each write operation of a certain field width to the variable size register, writing to the register object of the same width;

maintaining a record of which of the register objects contain valid data, which record is updated upon each write operation; and

for each read operation of a given field width, determining from the record whether there is valid data in more than one of the registers objects of the set which must be combined to give the same effect as the same read operation performed upon the variable size register; and

(a)   if it is determined that no combination is so required, reading directly from the appropriate register object; or

(b)   if it is determined that data from more than one register object must be so combined, combining the contents of those registers objects.

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9. (Previously presented) The method according to claim 48, wherein the step of determining whether or not the contents of more than one register object must be combined and if so which registers objects must be combined, is determined in accordance with the following conditions in respect of the set of associated register objects:

    (i)   if data required for an access to the variable size register lies wholly within a valid one of the register objects, the register object only is accessed; and

    (ii)   if the data required for an access lies within more than one of the register objects, data is combined from the more than one register objects to perform the access.

10. (Previously presented) A system for generating an intermediate representation of a register-based program code written for running on a programmable machine having a set of registers including at least one variable size register which is addressable by the program code in a plurality of different widths, the system comprising:

    means for generating a plurality of register objects each representing a respective one of the registers as referenced by the program code, wherein the at least one variable size register is represented by plural of the register objects with one the register object being provided for each different width of the variable size register; and

    means for generating a plurality of expression objects each representing a respective operator or operand according to the program code relating to the registers; and

    means for forming a network of the register objects and the expression objects, wherein each of the expression objects is referenced by one or more of the register objects to which it relates either directly, or indirectly via references from other of the expression objects.

11. (Previously presented) A system for generating an intermediate representation of program code expressed in terms of the instruction set of a subject processor comprising at least one variable size register which is accessible by the program code in a plurality of different field widths, the system comprising:

    means for generating a set of associated register objects each representing a different field width of the variable size register;

    means for writing, for each write operation of a certain field width to the variable size register, to the register object of the same width;

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means for maintaining a record of which the register objects contain valid data, the record being updated upon each write operation; and

means for determining from the record, for each read operation of a given field width, whether there is valid data in more than one of the associated set of register objects which must be combined to give the same effect as the same read operation performed upon the variable size register, and

(a)   if it is determined that no combination is so required, reading directly from the appropriate register object; or

(b)   if it is determined that data from more than one register objects must be so combined, combining the contents of those registers objects.

12. (Previously presented) The method of claim 1, wherein each of a plurality of variable size registers referenced by the program code is represented by a separately addressable subsets of the register objects.

13. (Previously presented) The method of claim 12, wherein each of the separately addressable subsets of the register objects concurrently represent the same respective variable size register.

14. (Cancelled)

15. (Previously presented) The method of claim 8, wherein each of a plurality of variable size registers referenced by the program code is represented by a separately addressable subsets of the register objects.

16. (Previously presented) The method of claim 15, wherein each of the separately addressable subsets of the register objects concurrently represent the same respective variable sized register.

17. (Cancelled)

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PAGE 27/41 * RCVD AT 3/15/2007 12:16:41 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/2 * DNIS:2739393 * CSID: * DURATION (mm-ss):10-34

18. (Previously presented) The method of claim 10, wherein each of a plurality of variable size registers referenced by the program code is represented by a separately addressable subsets of the register objects.

19. (Previously presented) The method of claim 18, wherein each of the separately addressable subsets of the register objects concurrently represent the same respective variable size register.

20. (Cancelled)

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21. (Previously presented) An emulation method of convert subject code into target code, comprising the computer-implemented steps of:

(a)   receiving the subject code expressed in an instruction set of a subject processor having at least one variable size register, wherein the variable size register is accessible by the subject code in a plurality of different width sub-fields overlaying part or all of a full width of the variable size register, and wherein the subject code includes at least write operations and read operations with respect to the variable size register;

(b)   generating an intermediate representation from the subject code, including performing the steps of:

generating a set of associated register objects each representing a different width sub-field of the variable size register;

representing each write operation in the subject code of a certain sub-field width to the variable size register, as a write operation to the register object of the same width and maintaining a record of which the register objects contain valid data, the record being updated upon each such write operation; and

representing each read operation in the subject code of a certain sub-field width from the variable size register, as a read operation from one or more of the register objects by determining from the record whether there is valid data in more than one of the associated set of register objects which must be combined to give the same effect as the same read operation performed upon the variable size register in the subject code, and

(i)   if it is determined that no combination is so required, reading directly from the appropriate register object; or

(ii)   if it is determined that data from more than one register objects must be so combined, combining the contents of those register objects; and

(c)   converting the intermediate representation into target code expressed in an instruction set of a target processor, including allocating the determined register objects to registers of the target processor and generating target code instructions which write to and read from the allocated target registers, according to the write operations and read operations defined in the intermediate representation.

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       In view of the above amendments, applicant believes the pending application is in condition for allowance.

                                       Respectfully submitted,

Dated:

_____
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